REMARKS

Claims 1-28 are pending. Claims 1, 11 and 12 have been amended, claims 7-10 have been canceled, and new claim 28 is added with this response. Claim 1 has been amended to include the limitations of provisionally allowable claims 9 and 10 and intervening claim 7. Reconsideration of the application is respectfully requested based on the following remarks.

I. ALLOWED SUBJECT MATTER

Applicant acknowledges with appreciation the allowance of claims 25-27 and the provisional allowance of claims 9-12. Accordingly, claim 1 has been amended to include the limitations of provisionally allowable claims 9 and 10 (expressed in the alternative) and intervening claim 7. Therefore claims 9 and 10 are cancelled. Claim 1 is now believed to be in condition for allowance. Moreover, claims 11 and 12 have been amended to depend from claim 1, and are also now believed to be in condition for allowance, and withdrawal of the objection is respectfully requested.

II. REJECTION OF CLAIMS 1-8 and 13-24 UNDER 35 U.S.C. § 102(e)

Claims 1-8 and 13-24 were rejected under 35 U.S.C. § 102(e), as being anticipated by U.S. Publication No. US 2004/00208314 A1 Patariu et al. (Patariu). Withdrawal of the rejection is respectfully requested for at least the following reasons.

As indicated above, Claim 1 has been amended to include the limitations of provisionally allowable claims 9 and 10 and intervening claim 7, thus claims 2-6 and 11-18 which depend therefrom are also now believed to be in condition for allowance.

i. Patariu does not teach or suggest a network interface device comprising a bus interface coupled with a host bus, and a media access control system coupled with the network and adapted to transfer data between the network interface device and the network as recited in claim 19.

Interface 506 of Fig. 5 of Patariu, as cited, can not adequately represent the bus interface (*e.g.*, 9 of Fig. 1E) of the present invention, as it is not ***coupled with a host bus in the host system*** (*e.g.*, 7) as recited in claim 19. Also, Memory 508 of Fig. 5 of Patariu, as cited, can not constitute the MAC system (*e.g.*, 10 of Fig. 1E) of the present invention, as it is not ***coupled between the network interface device*** (*e.g.*, 6) ***and the network*** (*e.g.*, 8) as recited in claim 19. Further, if CPU interface 506 of Fig. 5 of Patariu is cited to represent the bus interface (*e.g.*, 9 of Fig. 1E of the present invention), then Memory 508 of Fig. 5 of Patariu is not adapted to ***transfer data between the network interface device*** (comprising the bus interface 506) and the network. The network interface device of the present invention further comprises *a* ***single DES engine*** (*e.g.*, 5a) ***operable to perform 3DES processing by selectively feeding back intermediate data results to an input*** (*e.g.*, 5b) ***thereof...*** Patariu does not discuss or suggest feeding back intermediate data results to an input. Accordingly, not all features of independent claim 19 are disclosed by Patariu, and withdrawal of the rejection is respectfully requested.

ii. Patariu does not teach or suggest a method of 3DES processing comprising transferring data between the network interface device and the host system using a bus interface, transferring data utilizing a media access control system or performing security processing using a single DES engine as recited in claim 23.

The CPU interface 506 cited for Patariu in Fig. 5 can not represent the **bus interface** (*e.g.*, 9) of the network interface device (*e.g.*, 6 of Fig. 1E) of the present invention as the bus interface 506 which controls the bus, can not transfer data to the

host system (*e.g.*, 7) from this bus. Further, memory elements 508a and 508b can not represent the **media access control system** (*e.g.*, 10) as they do not control the transfer of data between a network interface device and a network. Finally, Patariu does not discuss **using a single DES engine** (*e.g.*, 5a) to perform security processing in a 3DES processing circuit.

Accordingly, not all features of independent claim 23 are disclosed by Patariu, and withdrawal of the rejection is respectfully requested.

III. NEW CLAIM, SAME SUBJECT MATTER

New claim 28 has been added, but is identical to previously presented claim 1, and thus does not require that a new search be made. Therefore entry of this claim is proper after final, and entry of the new claim is respectfully requested. Claim 28 (or the previously presented claim 1) is not believed to be anticipated by U.S. Publication No. US 2004/00208314 A1 Patariu et al. (Patariu) under 35 U.S.C. § 102(e), for at least the following reasons.

According to **MPEP § 2131:** *"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."*

Claim 28 comprises *a* ***select switch*** (*e.g.*, 24 of Fig. 1F of the present invention) ***coupled to*** *the data input (e.g., 26* of Fig. 1F*) of the security processing circuit, the data output (e.g., 23), and* ***the data input node*** *(e.g., 25* of Fig. 1F*)* ***of the single DES engine*** (*e.g.*, 5a of Fig. 1E or 21 of Fig. 1F), *the select switch adapted to selectively couple one of the data input (e.g., 26) and the intermediate result to the data input node of the single DES engine.* As will be shown below, the cited reference does not teach the above features.

i. Patariu does not teach or suggest a select switch having a connection to the data input node of the single DES engine essential for intermediate result processing as recited in claim 28.

Although Patariu (US Pub. US 2004/00208314 A1) is cited as having a select switch/Mux, item 210 of Fig. 2, this switch explicitly has **no connection** to the **data input node of the single DES engine** (*e.g.*, 5a of Fig. 1E or 21 of Fig. 1F), to provide "feedback" essential for **intermediate result processing** using a single DES engine. Thus, Patariu is also not **adapted to selectively couple one of the data input** *(e.g., 26* of Fig. 1F*)* and the **intermediate result to the data input node** *(e.g., 25* of Fig. 1F*)* of the single DES engine *(e.g., 21* of Fig. 1F*).* Mux 210 is not connected or adapted to *couple one of the data input and the intermediate result to the data input node of the engine* (DES or 3DES), and the Key & Encryption/Decryption Select (212 of Fig. 2 of Patariu) is not connected or coupled to the **data output** of the single DES engine (single DES or 3DES) as required of the **data select switch** of claim 28 (or the previously presented claim 1). Instead, Key & Encryption/Decryption Select 212 of Patariu is adapted to couple input data to the **keys input** of the 3DES block (208 of Fig. 2).

ii. Patariu does not teach or suggest a feedback path internal to the 3DES block engine essential for intermediate result processing as recited in claim 28.

The "feedback path" cited in Fig. 1 of Patariu between output FIFO block 110 and input FIFO block 108, ***is not a feedback path***, but is instead is described in paragraph [0032] of Patariu, as (similar to a bus) being under control of memory interface 106 to *transfer encrypted/decrypted data buffered in FIFO 110 to memory block 104*. Further, Patariu describes and illustrates a ***complete*** 3DES functional block (112 of Fig. 1 and 208 of Fig. 2), while the "feedback path" required in claim 28 (*a data input node adapted to process the intermediate result data from the data output during*

a second and third DES processing operation) between the select switch and *the* ***data input node*** of the ***single DES engine***, would be **internal** to this 3DES block 112, so cannot be the "feedback path" cited in Fig. 1 of Patariu.

iii. Patariu does not teach or suggest a single DES engine in combination with a select switch that is coupled to the data output and the data input node of the 3DES engine as recited in claim 28.

Claim 28 further comprises both **a single DES engine** (*e.g.*, 5a of Fig. 1E or 21 of Fig. 1F) **and a select switch coupled to the data output** and **the data input node**, which provides feedback therebetween for the intermediate result data. Instead, Patariu describes and illustrates a complete 3DES functional block (112 of Fig. 1) without this single DES engine feedback. Thus, the structure of Patariu appears to make no provision *to process the intermediate result data from the* ***data output*** *during a second and third DES processing operation* as recited in claim 28 (or the previously presented claim 1).

Accordingly, not all features of independent claim 28 are disclosed by Patariu, and favorable acceptance of this new claim is respectfully requested.

IV. CONCLUSION

For at least the above reasons, the claims currently under consideration are believed to be in condition for allowance.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 50-1733, AMDP783US.

Respectfully submitted,
ESCHWEILER & ASSOCIATES, LLC

By /Thomas G. Eschweiler/
Thomas G. Eschweiler
Reg. No. 36,981

National City Bank Building
629 Euclid Avenue, Suite 1000
Cleveland, Ohio 44114
(216) 502-0600